Effects of the Order of the CIC Filter on Decimation Filters for Sigma-Delta ADCs

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***Abstract*—Analog-to-digital converters (ADCs) play an important role at the boundary between the analog and digital domains. These converters, which are used in the majority of today's electronic systems, have two main goals: speed and precision. In addition, the power efficiency of these ADCs is very important. The sigma-delta ADC is currently one of the most accurate and consists of two main blocks: the sigma-delta modulator and the decimation filter. The filter usually consists of two or more parts, the first being a cascaded integrator-comb (CIC) filter which, in addition to attenuating the signal, also performs most of the overall filter decimation. The remaining cascade filters are usually stages of FIR filters whose main purpose is to attenuate the noise generated by the modulator. The CIC filter is responsible for a significant part of the decimation filter power consumption due to its high input data rate. This study presents the implementation and analysis of the order variation of a CIC filter for a sigma-delta ADC based on a third-order sigma-delta modulator. We show that power, area and speed are drastically affected by the order of the CIC filter, which underlines that the right choice of order is crucial for an optimized design.**

***Index Terms*—Sigma-delta, Modulator, CIC Filter, SNDR, ENOB.**

I. Introduction

Digital information technology is enabling the development of signal processing in medicine, manufacturing, aerospace and other fields. Most of the signal processing in electronic systems is digital, and the performance of the analog-to-digital converters (ADCs) at the boundaries of the digital domain becomes very important [1]. Recent applications in the fields of telecommunications, measurement, and consumer electronics require ever higher ADC resolution and speed [2]. In this context, sigma-delta converters are one of the most important in terms of resolution. However, progress must be made to enable an increase in speed and efficiency.

Sigma-Delta ($\Sigma\Delta$) ADCs are widely used in industry when high resolutions are required [3]. These converters consist of an oversampling modulator followed by a digital decimation filter, which generate a high-resolution output data-stream [3]. The main objective of the decimation filter is to attenuate the high-frequency noise generated by the noise-shaping while reducing the output data rate [4]. The block diagram of the Sigma-Delta ADC is shown in Figure 1.

While other kinds of ADCs have a single sample rate, the $\Sigma\Delta$ converter has two: the modulator sample rate (f_S) and the filter output data rate (f_D). The relationship between these two variables determines the oversampling of the modulator and consequently the decimation ratio, which is equal to the number of modulator samples per data output ($R = f_S/f_D$).

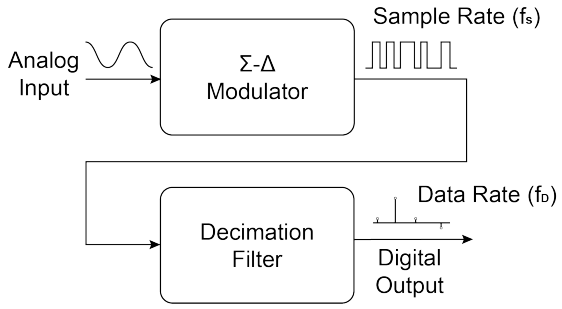

Fig. 1: Block diagram of a $\Sigma\Delta$ ADC.

The decimation filter is composed of three cascaded filters as shown in Figure 2. The first stage is a cascaded integrator-comb (CIC) filter; the second stage is a finite impulse response (FIR) compensation filter; and the last stage is a half-band FIR filter.

The complete decimation filter, depicted in Figure 2, was previously designed as described in [5]. In addition, the CIC filter was implemented using both Matlab in [6] and open source software in [7]. In this paper, the analysis of the CIC filter is revisited, investigating variations of its order and observing the resulting effects on the area and power consumption with respect to the frequency response characteristics. The variations of the CIC filter were designed in the Matlab working environment, encoded in System Verilog hardware description language, simulated using Modelsim, and synthesized using Cadence Genus tool in a standard 65 nm CMOS technology.

The remainder of this paper is organized as follows. Section II shows the sigma-delta modulator used to generate the CIC filter input data. Section III explains the CIC filter design. The analysis of CIC filter order is presented in Section IV. Section V presents the logical synthesis. Finally, some conclusions are drawn in Section VI.

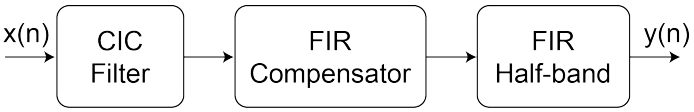

Fig. 2: Block diagram of a digital decimation filter.

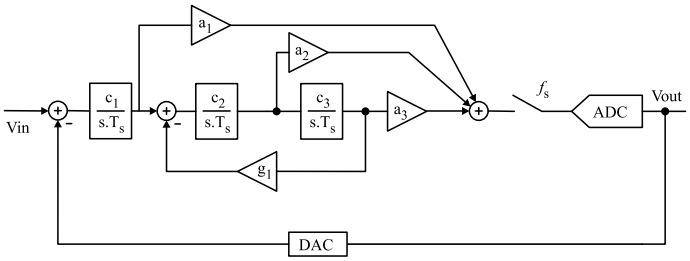

Fig. 3: Third-order continuous-time sigma-delta modulator.

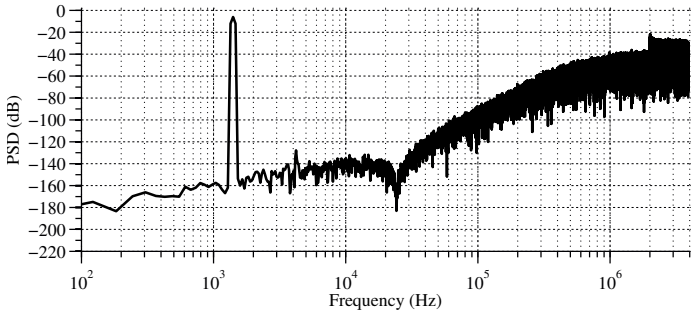

Fig. 4: PSD of the sigma-delta modulator.

II. Sigma-Delta Modulator

The simplified diagram of the modulator considered in this paper is presented in Figure 3. The modulator is a third-order single-bit continuous-time sigma-delta, with a sampling clock f_s of 8 MHz and a bandwidth BW of 31.25 kHz. The oversampling ratio (OSR) is defined as:

$$OSR = \frac{f_s}{2BW} \tag{1}$$

In this work the resulting oversampling ratio is 128. The power spectral density (PSD) at the modulator output is shown in Figure 4. For an input signal of -6.02 dBFS, the SNDR (signal-to-noise and distortion ratio) is 109 dB and the ENOB (effective number of bits) is 17.81 bits.

The bandpass of the decimation filter is 20 kHz and the transition band is 11.25 kHz, resulting in a stopband that starts at 31.25 kHz. The digital filter shown in Figure 2 performs a decimation ratio of 128, decimating by 32 in the CIC filter and by 2 in each of the FIR stages.

III. CIC Filter

Cascaded integrator-comb digital filters are computationally efficient implementations of narrowband low-pass filters and are often embedded in hardware implementations of decimation, interpolation and $\Sigma\Delta$ converter filtering [8]. These applications are associated with high data rate filtering and $\Sigma\Delta$ ADC and DAC converters. The CIC filters originate from the concept of a recursive running sum filter [9], which makes them an efficient form of a non-recursive moving average filter. A very important feature of the CIC is that although it can be implemented recursively, it has guaranteed stability and linear phase due to its finite impulse responses.

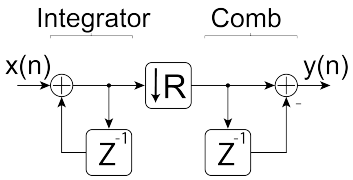

Fig. 5: First order decimation cascaded integrator-comb filter.

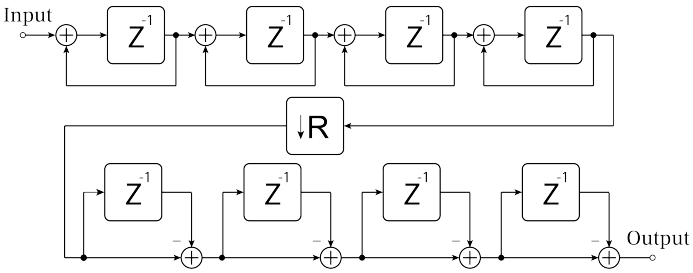

Fig. 6: Fourth-order pipeline CIC filter.

The transfer function of a decimated CIC filter of order Lth can be expressed either in recursive or in non-recursive form as given by

$$\begin{aligned} H(z) &= \left[\frac{1-z^{-R}}{1-z^{-1}}\right]^L \\ &= \left[\sum_{n=0}^{R-1} z^{-n}\right]^L \\ &= (1+z^{-1}+z^{-2}+\cdots+z^{-R+1})^L \end{aligned} \tag{2}$$

where R is the decimation factor and L is the filter order. Figure 5 shows a first-order CIC filter, which can be considered a recursive filter due to the feedback present in the integrator.

One way to achieve a high-speed CIC filter is to implement the pipeline filter structure [10]. Figure 6 shows this topology, in which energy consumption is reduced because the switching time in the stages before decimation is reduced, i.e. data transfer takes place at a faster clock rate.

The CIC filter implemented in this work presents the pipeline structure shown in Figure 6. Increasing the order of the filter implies cascading an integrator block and a comb. The transfer function represented by this implementation is the same as that shown in equation 2, with $R = 32$ and L ranging between 4, 5 and 6.

In addition to the use of more integration and comb blocks, the increase in the order of the CIC filter also leads to an increase in the word length of the individual blocks. The word length (W) of the filter varies depending on the order and decimation and can be calculated using the following expression:

$$W = W_{in} + L\log_2(R) \tag{3}$$

where W_{in} is the length of the input word, R is the decimation and L is the order. In this work, $W_{in} = 2$, $R = 32$ and L ranges from 4 to 6. As a result, the word length of the CIC filter is 22, 27 and 32 for orders 4, 5 and 6, respectively.

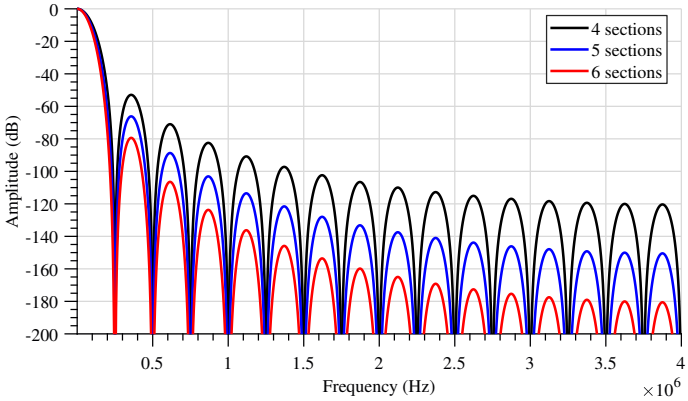

Fig. 7: CIC filter attenuation.

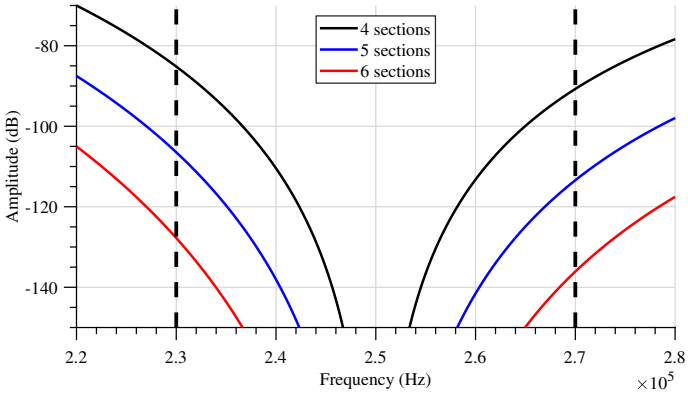

Fig. 8: CIC filter worst case of alias rejection.

Increasing the word length significantly increases the area and power consumption of the CIC filter. This effect should be taken into account when choosing the order of the filter.

IV. Analysis of Order of the CIC Filter

The main objective of increasing the order of the CIC filter is to improve alias rejection. The alias frequencies occur at multiples of the CIC filter output data rate, as can be seen in Figure 7. This figure also shows that a higher order results in greater attenuation of high-frequency noise.

It can be seen that the worst attenuation of the alias occurs around the frequency of 250 kHz. This region is shown in detail in Figure 8, where the dashed lines represent the limit of the alias frequencies for a passband of 20 kHz. As the filter order increases, the attenuation increases around the center frequency of 250 kHz. Figure 8 can also be used as a guide for selecting the best order of the CIC filter according to the desired alias rejection.

Figure 9 shows that the CIC filter causes an attenuation in the passband that increases with order. This drop is corrected with an FIR filter for compensation, as shown in Figure 2. Despite the increase in attenuation, it is not necessary to increase the order of the compensating FIR filter with the increase in the order of the CIC, only its coefficients are recalculated.

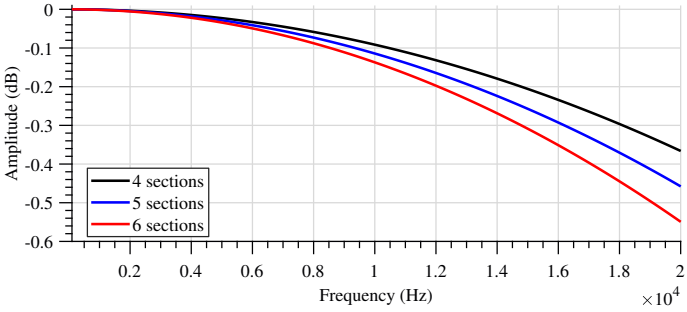

Fig. 9: Magnitude drop in the passband for the CIC filter of orders 4, 5, and 6.

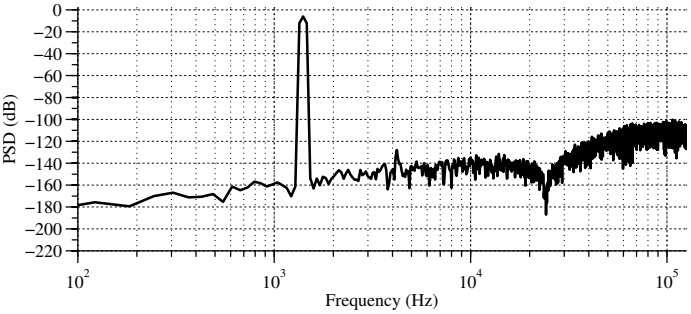

Fig. 10: PSD of a fourth-order CIC filter.

The PSD of the output signal of the fourth-order CIC filter is shown in Figure 10. With an SNDR of 108.97 dB and an ENOB of 17.8, the results are almost identical to those of the modulator. The PSD results for the other orders of the CIC filter were omitted as the results were virtually identical. As expected, it can be seen in Figure 10 that some of the high frequency noise is removed and the alias rejection is sufficient to avoid significant performance degradation.

V. CIC Filter Logic Synthesis

To perform the logic synthesis, three different scenarios were considered: the fastest, the slowest and the typical case. For the fastest scenario, a voltage of 1.32 V and a temperature of $-40°$C were assumed. For the worst-case (slowest) scenario, a voltage of 1.08 V and a temperature of $125°$C were taken into account. For the typical case, the analysis was based on a nominal supply voltage of 1.2 V and a temperature of $25°$C. Table I shows the results of this analysis and the previously results of the signal power spectrum.

The power consumption results for the typical case increases with the order of the filter. The fifth-order filter shows an increase of 53.21% compared to the fourth-order filter, while

TABLE I: Results obtained for area, power consumption and delay after logic synthesis.

Order	4^{th}	5^{th}	6^{th}
Gate Area (μm^2)	2821	4211	5885
Power consumption (μW)	35.047	53.736	77.506
Critical path delay (ns)	7.413	9.325	11.234

TABLE II: Evaluation of the effect of the order of the CIC filter on the decimation filter.

Order	4^{th}	5^{th}	6^{th}
Typical Power Decimation Filter (μW) [5]	165.03	183.72	207.49
Typical Power CIC Fitter (%)	21.24%	29.25%	37.35%
Area Decimation Filter (μm^2) [5]	12879	14269	15943
Area CIC Filter (%)	21.90%	29.51%	36.91%

the sixth-order filter shows an increase of 108.64% compared to the fourth-order filter.

The area also increases with the order of the filter, which was to be expected due to the need for more logic blocks in the filter. The fifth-order filter is 53.29% larger than the fourth-order filter and the sixth-order filter is 121.27% larger.

The critical path delay is analyzed in nanoseconds, and only the worst case corner is considered. The fifth and sixth order filters have a 25.78% and 51.54% larger critical path delay compared to the fourth order filter, respectively.

Table II presents the logic synthesis results for the decimation filter shown in Figure 2, which is used in the modulator shown in Figure 3 [5]. This table can be used to evaluate the effects of increasing the order of the CIC filter on the decimation filter.

The increase in area and power consumption of the CIC filter shows a linear behavior corresponding to the increase in the order of the filter. However, to increase the attenuation of the first harmonic of the signal, a higher order CIC filter is required. The choice of the order of the filters should be evaluated taking into account the specifications of the design.

Analysis of the results shows that the sixth-order filter consumes more than twice as much area and power as the fourth-order filter, and that the delay in the critical path increases significantly. In contrast, comparing the area and power of the decimation filter shows an increase of 15.01% and 16.16%, respectively. Table I shows that the results for area, power and critical path delay increase almost linearly with the filter order. Thus, the right choice of the order of the CIC filter can lead to significant savings in power consumption and area while improving speed considerably.

VI. Conclusion

This paper presented the operation of decimation filters used in sigma-delta ADCs, focusing on the CIC filter, an important filter used to reduce the sampling rate of a signal. Analyzes were performed by varying the filter order and observing the increase in signal attenuation, decimation and signal word length. It was shown that the order of the CIC filters can be determined by the alias rejection, which is crucial to avoid performance degradation in a high noise environment. Finally, a logical synthesis was performed, where it was found that the area, power consumption and critical path delay increase linearly with the order of the filter. However, the most significant effect is in the area and power consumption.

In this paper, analyzes were presented by varying the order of the CIC filter, but no analyzes were performed by changing the decimation of the filter, as this would change the specifications of the design. Increasing The increase in the order of the CIC filter leads to a stronger attenuation of the high frequency noise. The effects on the area and power on the decimation filter with increasing the order of the CIC filter were also evaluated.

This analysis is very important because the non-optimal sizing of the CIC filter can significantly affect the performance of the decimation filter. Future work is aimed at further optimizing the CIC filter, implementing the filter non-recursively, and analyzing the effects on the decimation filter in general, as well as investigating the area and power parameters.

Acknowledgments

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